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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/627,976	07/28/2003	Anne Kaszynski	T2147-908627	4095

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EXAMINER	
ALHIJA, SAIF A	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 10/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/627,976	KASZYNSKI ET AL.	
	Examiner	Art Unit	
	Saif A. Alhija	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/25/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 21-47 have been presented for examination.

PRIORITY

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 25 March 2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the Examiner has considered the IDS as to the merits.

Drawings Objections

4. The drawings are objected to because they contain French language labels with hand written English definitions. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

MPEP 2106 recites:

> The claimed invention as a whole must accomplish a practical application. That is, it must produce a "useful, concrete and tangible result" State Street 149 F.3d at 1373, 47 USPQ2d at 1601-02. A process that consists solely of the manipulation of an abstract idea is not concrete or tangibles. See In re Warmerdam, 33 F.3d 1354, 1360, 31 USPQ2d 1754, 1759 (Fed.Cir. 1994). See also Schrader, 22 F.3d at 295, 30 USPQ2d at 1459.

5. **Claims 21-37, 39-42, 44, and 46-47 are rejected** under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

i) The claims recite creating a transmission mode, integrating a software model, and utilizing a verification platform. These steps appear to be a manipulation of data and/or software modules. It is unclear if the resultant of the claims is stored, provided to a user, etc. As such the claims do not produce a useful, concrete, and tangible result.

ii) The claims appear to recite a computer program. It should be noted that code (i.e., a computer software program) does not do anything per se. Instead, it is the code stored on a computer that, *when executed*, instructs the computer to perform various functions. The following claim is a generic example of a proper computer program product claim;

A computer program product embodied on a computer-readable medium and comprising code that, when executed, causes a computer to perform the following:

Function A
Function B
Function C, etc...

All claims dependent upon a rejected base claim are rejected by virtue of their dependency.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. **Claim 32 is rejected** under 35 U.S.C. 112, first paragraph, for undue breadth. The claim contains a single means and is therefore nonenabling for the scope of the claim because the specification disclosed at most only those means known to the inventor. See MPEP 2164.08(a).

Claims 33-27 are rejected by virtue of their dependency.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. **Claims 21-47 are rejected** under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

i) The claims are generally narrative and indefinite, failing to conform with current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors. As such it is difficult to ascertain the complete scope and meaning of the claims.

Claim Objections

8. As stated in MPEP Section 2143.03. A claim limitation which is considered indefinite cannot be disregarded. If a claim is subject to more than one interpretation, at least one of which would render the claim unpatentable over the prior art, the examiner should reject the claim as indefinite under 35 U.S.C. 112, second paragraph (see MPEP § 706.03(d)) and should reject the claim over the prior art based on the interpretation of the claim that renders the prior art applicable. Ex parte Ionescu, 222 USPQ 537 (Bd.

Pat. App. & Inter. 1984) (Claims on appeal were rejected on indefiniteness grounds only; the rejection was reversed and the case remanded to the examiner for consideration of pertinent prior art.). Compare In re Wilson, 424 F.2d 1382, 165 USPQ 494 (CCPA 1970) (if no reasonably definite meaning can be ascribed to certain claim language, the claim is indefinite, not obvious) and In re Steele, 305 F.2d 859,134 USPQ 292 (CCPA 1962) (it is improper to rely on speculative assumptions regarding the meaning of a claim and then base a rejection under 35 U.S.C. 103 on these assumptions).

9. Claim 21 is objected to because of the following informalities:

Claim 21 contains a period before the end of the claim, specifically after the phrase transmission mode. See MPEP 608.01(m), "Each claim begins with a capital letter and ends with a period. Periods may not be used elsewhere in the claims except for abbreviations. See Fressola v. Manbeck, 36 USPQ2d 1211 (D.D.C. 1995)."

10. Claim 45 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The claim ends with "to be applied to the."

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. **Claims 21-47 are rejected** under 35 U.S.C. 102(e) as being clearly anticipated by **Killian et al. "Automated Processor Generation System for Designing a Configurable Processor and Method for the Same", U.S. Patent No. 6,477,683, hereafter referred to as Killian.**

12. **Claims 21-47 are rejected** under 35 U.S.C. 102(e) as being clearly anticipated by **Lin et al. "Converification System and Method", U.S. Patent No. 6,389,379, hereafter referred to as Lin.**

Regarding Claim 21:

The references disclose A method for on demand functional verification of a software model (40) of an application specific integrated circuit (ASIC), wherein said software model is written in a low–level programming language and separately causes a model of the circuit to be generated and debugging of functional verification tests to be applied to the model of the circuit for constituting a verification platform, comprising a transmission mode and a verification mode:

creating in the transmission mode an autonomous circuit emulator (1), obtained by replacing the software model (40) which is in a low level programming language physically describing the circuit under design to be validated with a high level language abstract description generating response data structures in accordance with a functional specification (20) of the project as a function of the stimuli received, this mode being called the "transmission mode."

integrating the software model in a verification mode into a verification platform and connecting previously validated autonomous circuit emulator, in parallel, to interfaces of the software model of the circuit, and to an environment emulator; and

utilizing the verification platform as a reference for the validation of response data transmitted by the software model of the circuit.

(Claim Interpretation. Co-Simulation of an ASIC utilizing high and low level programming languages)

(Killian. Abstract. Figures 1, 6 , 8, and 10 and their corresponding descriptions. Column 2, Lines 12-23. Column 3, Lines 1-10. Column 8, Lines 9-43. Column 9, Line 37 – Column 10, Line 67. Column 23, Lines 21-45)

(Lin. Abstract. Figures 1-6, 10 and 16 and their corresponding descriptions. Column 18, Lines 1 – Column 19, Line 4. Column 21, Line 34 – Column 22, Line 11. Column 27, Line 45 – Column 28, Line 57. Column 57, Line 17-35)

Regarding Claim 22:

The references disclose A method according to claim 21, wherein a user:

generates, using a data processing system, the autonomous circuit emulator (1) which provides a simulation configuration

corresponding to the software model (40) of the ASIC using the functional specification (20),

writes, from the functional specification (20), and stores in a test platform (21, 22, 23) for integrated circuit models, a program (51) for

testing the software model (40) of the ASIC, comprising input stimuli sequences to be provided to the software model (40) of the ASIC, which

the autonomous simulation configuration (1), based on the functional specification (20), corresponds to output stimuli sequences,

links together, and activates, the autonomous simulation configuration (1) and the test platform (21, 22, 23), and

observes the output stimuli of the HDL-type model (40) of the ASIC in order to functionally validate the system constituted by the

software model of the ASIC circuit and the validation test program (210),and thus validates the software model (40) in comparison to the functional specification (20) .

(Claim Interpretation. Co-Simulation/emulation of an ASIC utilizing high and low level programming languages with functional verification)

(Killian. Abstract. Figures 1, 6 , 8, and 10 and their corresponding descriptions. Column 2, Lines 12-23. Column 3, Lines 1-10. Column 8, Lines 9-43. Column 9, Line 37 – Column 10, Line 67. Column 23, Lines 21-45)

(Lin. Abstract. Figures 1-6, 10 and 16 and their corresponding descriptions. Column 18, Lines 1 – Column 19, Line 4. Column 21, Line 34 – Column 22, Line 11. Column 27, Line 45 – Column 28, Line 57. Column 57, Line 17-35)

Regarding Claim 23:

The references disclose A method according to claim 21, wherein the autonomous configuration (1) communicates with the user to control the activation of previously created and stored models of input stimuli sequences defined in a high-level programming language, and controls the activation of associated programs (90) for the progressive validation of test sequences determined from the models.

(Claim Interpretation. User control and testing)

(Killian. Abstract. Figures 1, 6 , 8, and 10 and their corresponding descriptions. Column 2, Lines 12-23. Column 3, Lines 1-10. Column 8, Lines 9-43. Column 9, Line 37 – Column 10, Line 67. Column 23, Lines 21-45)

(Lin. Abstract. Figures 1-6, 10 and 16 and their corresponding descriptions. Column 18, Lines 1 – Column 19, Line 4. Column 21, Line 34 – Column 22, Line 11. Column 27, Line 45 – Column 28, Line 57. Column 57, Line 17-35)

Regarding Claim 24:

The references disclose A method according to claim 21, wherein a user writes and provides the functional specification (20) in a low-level programming language, specifying functional models of circuits.

(Claim Interpretation. User testing utilizing functional input)

(Killian. Abstract. Figures 1, 6 , 8, and 10 and their corresponding descriptions. Column 2, Lines 12-23. Column 3, Lines 1-10. Column 8, Lines 9-43. Column 9, Line 37 – Column 10, Line 67. Column 23, Lines 21-45)

(Lin. Abstract. Figures 1-6, 10 and 16 and their corresponding descriptions. Column 18, Lines 1 – Column 19, Line 4. Column 21, Line 34 – Column 22, Line 11. Column 27, Line 45 – Column 28, Line 57. Column 57, Line 17-35)

Regarding Claim 25:

The references disclose A method according to claim 22, wherein the user writes and provides the functional specification (20) in a low-level programming language, specifying functional models of circuits.

(Claim Interpretation. User testing utilizing functional input)

(Killian. Abstract. Figures 1, 6 , 8, and 10 and their corresponding descriptions. Column 2, Lines 12-23. Column 3, Lines 1-10. Column 8, Lines 9-43. Column 9, Line 37 – Column 10, Line 67. Column 23, Lines 21-45)

(Lin. Abstract. Figures 1-6, 10 and 16 and their corresponding descriptions. Column 18, Lines 1 – Column 19, Line 4. Column 21, Line 34 – Column 22, Line 11. Column 27, Line 45 – Column 28, Line 57. Column 57, Line 17-35)

Regarding Claim 26:

The references disclose A method according to claim 23, wherein a user writes and provides the functional specification (20) in a low-level programming language, specifying functional models of circuits.

(Claim Interpretation. User testing utilizing functional input)

(Killian. Abstract. Figures 1, 6 , 8, and 10 and their corresponding descriptions. Column 2, Lines 12-23. Column 3, Lines 1-10. Column 8, Lines 9-43. Column 9, Line 37 – Column 10, Line 67. Column 23, Lines 21-45)

(Lin. Abstract. Figures 1-6, 10 and 16 and their corresponding descriptions. Column 18, Lines 1 – Column 19, Line 4. Column 21, Line 34 – Column 22, Line 11. Column 27, Line 45 – Column 28, Line 57. Column 57, Line 17-35)

Regarding Claim 27:

The references disclose A method according to claim 21, wherein a user provides the functional specification (20), in the form of a program in a low level programming language of functional models of circuits, and a program in a high level programming language of functional models of circuits, and the user controls the autonomous simulation configuration (1) so as to perform a co-simulation by synchronizing the execution of the two specification programs.

(Claim Interpretation. Co-simulation and synchronization)

(Killian. Abstract. Figures 1, 6 , 8, and 10 and their corresponding descriptions. Column 2, Lines 12-23. Column 3, Lines 1-10. Column 8, Lines 9-43. Column 9, Line 37 – Column 10, Line 67. Column 23, Lines 21-45)

(Lin. Abstract. Figures 1-6, 10 and 16 and their corresponding descriptions. Column 18, Lines 1 – Column 19, Line 4. Column 21, Line 34 – Column 22, Line 11. Column 27, Line 45 – Column 28, Line 57. Column 57, Line 17-35)

Regarding Claim 28:

The references disclose A method according to claim 27 wherein the low level language is an HDL type and the high level language C++.

(Killian. Abstract. Figures 1, 6 , 8, and 10 and their corresponding descriptions. Column 2, Lines 12-23. Column 3, Lines 1-10. Column 8, Lines 9-43. Column 9, Line 37 – Column 10, Line 67. Column 23, Lines 21-45)

(Lin. Abstract. Figures 1-6, 10 and 16 and their corresponding descriptions. Column 18, Lines 1 – Column 19, Line 4. Column 21, Line 34 – Column 22, Line 11. Column 27, Line 45 – Column 28, Line 57. Column 57, Line 17-35)

Regarding Claim 29:

The references disclose A method according to claim 21 wherein the verification platform verifies that the responses of the software model of the ASIC are within response time ranges specified in the functional specification (20).

(Claim Interpretation. Timing verification)

(Killian. Abstract. Figures 1, 6 , 8, and 10 and their corresponding descriptions. Column 2, Lines 12-23. Column 3, Lines 1-10. Column 8, Lines 9-43. Column 9, Line 37 – Column 10, Line 67. Column 23, Lines 21-45)

(Lin. Abstract. Figures 1-6, 10 and 16 and their corresponding descriptions. Column 18, Lines 1 – Column 19, Line 4. Column 21, Line 34 – Column 22, Line 11. Column 27, Line 45 – Column 28, Line 57. Column 57, Line 17-35)

Regarding Claim 30:

The references disclose A method according to claim 22 wherein the verification platform verifies that the responses of the software model of the ASIC are within response time ranges specified in the functional specification (20).

(Claim Interpretation. Timing verification)

(Killian. Abstract. Figures 1, 6 , 8, and 10 and their corresponding descriptions. Column 2, Lines 12-23. Column 3, Lines 1-10. Column 8, Lines 9-43. Column 9, Line 37 – Column 10, Line 67. Column 23, Lines 21-45)

(Lin. Abstract. Figures 1-6, 10 and 16 and their corresponding descriptions. Column 18, Lines 1 – Column 19, Line 4. Column 21, Line 34 – Column 22, Line 11. Column 27, Line 45 – Column 28, Line 57. Column 57, Line 17-35)

Regarding Claim 31:

The references disclose A method according to claim 23 wherein the verification platform verifies that the responses of the software model of the ASIC are within response time ranges specified in the functional specification (20).

(Claim Interpretation. Timing verification)

(Killian. Abstract. Figures 1, 6 , 8, and 10 and their corresponding descriptions. Column 2, Lines 12-23. Column 3, Lines 1-10. Column 8, Lines 9-43. Column 9, Line 37 – Column 10, Line 67. Column 23, Lines 21-45)

(Lin. Abstract. Figures 1-6, 10 and 16 and their corresponding descriptions. Column 18, Lines 1 – Column 19, Line 4. Column 21, Line 34 – Column 22, Line 11. Column 27, Line 45 – Column 28, Line 57. Column 57, Line 17-35)

Regarding Claim 32:

The references disclose A verification platform for on demand verification of a software model of an integrated circuit (ASIC), characterized in that it comprises data processing means that allow a client to select test models producing input stimuli for the ASIC, said data processing means being constructed and arranged to read functional specification elements (20) of the ASIC and comprising programs (90) that form an emulator and generate a functional validation test program (51) constituted by output stimuli, from the input stimuli and the functional specification elements (20).

(Claim Interpretation. Co-Simulation/Emulation of an ASIC utilizing high and low level programming languages)

(Killian. Abstract. Figures 1, 6 , 8, and 10 and their corresponding descriptions. Column 2, Lines 12-23. Column 3, Lines 1-10. Column 8, Lines 9-43. Column 9, Line 37 – Column 10, Line 67. Column 23, Lines 21-45)

(Lin. Abstract. Figures 1-6, 10 and 16 and their corresponding descriptions. Column 18, Lines 1 – Column 19, Line 4. Column 21, Line 34 – Column 22, Line 11. Column 27, Line 45 – Column 28, Line 57. Column 57, Line 17-35)

Regarding Claim 33:

The references disclose A verification platform according to claim 32, comprising a library of functional models of circuit blocks for ASICs and means for selecting models through a definition file of

the integrated circuit configuration, in order to create a model corresponding to the functional specification of the ASIC that is integrated into the definition of its environment.

(Claim Interpretation. Definition Library defining the IC)

(Killian. Abstract. Figures 1, 6 , 8, and 10 and their corresponding descriptions. Column 2, Lines 12-23. Column 3, Lines 1-10. Column 8, Lines 9-43. Column 9, Line 37 – Column 10, Line 67. Column 23, Lines 21-45)

(Lin. Abstract. Figures 1-6, 10 and 16 and their corresponding descriptions. Column 18, Lines 1 – Column 19, Line 4. Column 21, Line 34 – Column 22, Line 11. Column 27, Line 45 – Column 28, Line 57. Column 57, Line 17-35)

Regarding Claim 34:

The references disclose A verification platform according to claim 32, further including, in a link connecting the platform to a client, two serial programming language adaptation circuits (11, 12), that transform commands in a high level programming language (C++), used by the client, into commands in a low level programming language used by the ASIC model, and respectively, to the commands in the low level programming language back into commands in a high level programming language.

(Claim Interpretation. Process communications)

(Killian. Abstract. Figures 1, 6 , 8, and 10 and their corresponding descriptions. Column 2, Lines 12-23. Column 3, Lines 1-10.)

(Lin. Abstract. Figures 28-30 and their corresponding descriptions. Column 87, Line 50-64)

Regarding Claim 35:

The references disclose A verification platform according to claim 32, characterized in that the platform includes means (90, 10) for executing operations at the same time as the simulation and upon detection of an error interrupting operations at the very moment the error appears.

(Claim Interpretation. Error detection)

(Killian. Abstract. Figures 1, 6 , 8, and 10 and their corresponding descriptions. Column 2, Lines 12-23. Column 3, Lines 1-10. Column 8, Lines 9-43. Column 9, Line 37 – Column 10, Line 67. Column 23, Lines 21-45)

(Lin. Abstract. Figures 1-6, 10 and 16 and their corresponding descriptions. Column 18, Lines 1 – Column 19, Line 4. Column 21, Line 34 – Column 22, Line 11. Column 27, Line 45 – Column 28, Line 57. Column 57, Line 17-35)

Regarding Claim 36:

The references disclose A verification platform according to claim 32, characterized in that the function specification elements are constituted by a truth table corresponding to the functions of the various functional circuit elements of the ASIC software model (40), and a propagation delay to be respected between each input and each output.

(Claim Interpretation. Truth Table Analysis)

(Killian. Abstract. Figures 1, 6 , 8, and 10 and their corresponding descriptions. Column 2, Lines 12-23. Column 3, Lines 1-10. Column 8, Lines 9-43. Column 9, Line 37 – Column 10, Line 67. Column 23, Lines 21-45)

(Lin. Abstract. Figures 1-6, 10 and 16 and their corresponding descriptions. Column 18, Lines 1 – Column 19, Line 4. Column 21, Line 34 – Column 22, Line 11. Column 27, Line 45 – Column 28, Line 57. Column 57, Line 17-35)

Regarding Claim 37:

The references disclose A verification platform according to claim 32, characterized in that the functional specification elements (20) are constituted by a behavior table corresponding to the functions of the various functional circuit elements of the ASIC software model (40), and a propagation delay to be respected between each input and each output.

(Claim Interpretation. Behavioral Analysis)

(Killian. Abstract. Figures 1, 6 , 8, and 10 and their corresponding descriptions. Column 2, Lines 12-23. Column 3, Lines 1-10. Column 8, Lines 9-43. Column 9, Line 37 – Column 10, Line 67. Column 23, Lines 21-45)

(Lin. Abstract. Figures 1-6, 10 and 16 and their corresponding descriptions. Column 18, Lines 1 – Column 19, Line 4. Column 21, Line 34 – Column 22, Line 11. Column 27, Line 45 – Column 28, Line 57. Column 57, Line 17-35)

Regarding Claim 38:

The references disclose A verification platform according to claim 32, further including a cache memory (962) for storing the blocks used by nodes according to node addresses, and means for managing, for an address used by one or more nodes, a presence vector with one presence indicator per node.

(Claim Interpretation. Nodal Analysis)

(Killian. Abstract. Figures 1, 6 , 8, and 10 and their corresponding descriptions. Column 2, Lines 12-23. Column 3, Lines 1-10. Column 8, Lines 9-43. Column 9, Line 37 – Column 10, Line 67. Column 23, Lines 21-45)

(Lin. Abstract. Figures 1-6, 10 and 16 and their corresponding descriptions. Column 18, Lines 1 – Column 19, Line 4. Column 21, Line 34 – Column 22, Line 11. Column 27, Line 45 – Column 28, Line 57. Column 57, Line 17-35)

Regarding Claim 39:

The references disclose A verification platform according to claim 38 characterized in that the programs (90) are object-oriented and the emulator is structured as a set of classes for managing a collection of execution hypotheses for a transaction in a memory block of the software model, and for managing transactions that are concurrently colliding using the same memory block.

(Claim Interpretation. Transaction analysis)

(Killian. Abstract. Figures 1, 6 , 8, and 10 and their corresponding descriptions. Column 2, Lines 12-23. Column 3, Lines 1-10. Column 8, Lines 9-43. Column 9, Line 37 – Column 10, Line 67. Column 23, Lines 21-45)

(Lin. Abstract. Figures 1-6, 10 and 16 and their corresponding descriptions. Column 18, Lines 1 – Column 19, Line 4. Column 21, Line 34 – Column 22, Line 11. Column 27, Line 45 – Column 28, Line 57. Column 57, Line 17-35)

Regarding Claim 40:

The references disclose A verification platform according to claim 38, characterized in that algorithms of the programs (9) of the emulator perform the following functions: generating predictions, eliminating predictions, readjusting incorrect predictions, reducing the number of valid hypotheses, and terminating collisions.

(Claim Interpretation. Prediction generation)

(Killian. Abstract. Figures 1, 6 , 8, and 10 and their corresponding descriptions. Column 2, Lines 12-23. Column 3, Lines 1-10. Column 8, Lines 9-43. Column 9, Line 37 – Column 10, Line 67. Column 23, Lines 21-45)

(Lin. Abstract. Figures 1-6, 10 and 16 and their corresponding descriptions. Column 18, Lines 1 – Column 19, Line 4. Column 21, Line 34 – Column 22, Line 11. Column 27, Line 45 – Column 28, Line 57. Column 57, Line 17-35)

Regarding Claim 41:

The references disclose A verification platform according to claim 40, characterized in that the emulator of the circuit generates predictions without having to obtain additional information on the internal operation of the circuit under design.

(Claim Interpretation. Testing utilizing functional input)

(Killian. Abstract. Figures 1, 6 , 8, and 10 and their corresponding descriptions. Column 2, Lines 12-23. Column 3, Lines 1-10. Column 8, Lines 9-43. Column 9, Line 37 – Column 10, Line 67. Column 23, Lines 21-45)

(Lin. Abstract. Figures 1-6, 10 and 16 and their corresponding descriptions. Column 18, Lines 1 – Column 19, Line 4. Column 21, Line 34 – Column 22, Line 11. Column 27, Line 45 – Column 28, Line 57. Column 57, Line 17-35)

Regarding Claim 42:

The references disclose A verification platform according to claim 38, characterized in that the platform is used as an emulator of a router circuit, a circuit with cache or a router circuit with cache.

(Claim Interpretation. The "emulator of a router circuit, a circuit with cache or a router circuit with cache" **are intended uses of the verification platform and as such carry no patentable weight.)**

(Killian. Abstract. Figures 1, 6 , 8, and 10 and their corresponding descriptions. Column 2, Lines 12-23. Column 3, Lines 1-10. Column 8, Lines 9-43. Column 9, Line 37 – Column 10, Line 67. Column 23, Lines 21-45)

(Lin. Abstract. Figures 1-6, 10 and 16 and their corresponding descriptions. Column 18, Lines 1 – Column 19, Line 4. Column 21, Line 34 – Column 22, Line 11. Column 27, Line 45 – Column 28, Line 57. Column 57, Line 17-35)

Regarding Claim 43:

The references disclose A verification platform according to claim 38 for testing a software model of an integrated circuit (ASIC) on demand characterized in that the platform comprises an ASIC emulator (1) for controlling a comparator (23) that receives values generated by a software model of the ASIC circuit tested, upon reception of stimuli sent by at least one stimuli generating circuit (21) storing a test program, an interface (11) for translating the stimuli from an advanced language into a low level language corresponding to that of the software model, and means for validating the verification in case of the detection of a collision by the comparator.

(Claim Interpretation. Testing utilizing functional input)

(Killian. Abstract. Figures 1, 6 , 8, and 10 and their corresponding descriptions. Column 2, Lines 12-23. Column 3, Lines 1-10. Column 8, Lines 9-43. Column 9, Line 37 – Column 10, Line 67. Column 23, Lines 21-45)

(Lin. Abstract. Figures 1-6, 10 and 16 and their corresponding descriptions. Column 18, Lines 1 – Column 19, Line 4. Column 21, Line 34 – Column 22, Line 11. Column 27, Line 45 – Column 28, Line 57. Column 57, Line 17-35)

Regarding Claim 44:

The references disclose A verification platform according to claim 38, further comprising means for selecting the response to stimuli that depend on the composition of the circuits tested, said means for selecting being constituted by a model generated by means for selecting functional models from a library,

which associates with each of the models the responses to a given stimulus, the model corresponding to the composition of the circuit to be tested.

(Claim Interpretation. Testing utilizing functional input)

(Killian. Abstract. Figures 1, 6 , 8, and 10 and their corresponding descriptions. Column 2, Lines 12-23. Column 3, Lines 1-10. Column 8, Lines 9-43. Column 9, Line 37 – Column 10, Line 67. Column 23, Lines 21-45)

(Lin. Abstract. Figures 1-6, 10 and 16 and their corresponding descriptions. Column 18, Lines 1 – Column 19, Line 4. Column 21, Line 34 – Column 22, Line 11. Column 27, Line 45 – Column 28, Line 57. Column 57, Line 17-35)

Regarding Claim 45:

The references disclose A verification platform according to claim 44, further including means (7) for storing responses selected so as to create a test model (70) to be applied to the

(Claim Interpretation. Storage)

(Killian. Abstract. Figures 1, 6 , 8, and 10 and their corresponding descriptions. Column 2, Lines 12-23. Column 3, Lines 1-10. Column 8, Lines 9-43. Column 9, Line 37 – Column 10, Line 67. Column 23, Lines 21-45)

(Lin. Abstract. Figures 1-6, 10 and 16 and their corresponding descriptions. Column 18, Lines 1 – Column 19, Line 4. Column 21, Line 34 – Column 22, Line 11. Column 27, Line 45 – Column 28, Line 57. Column 57, Line 17-35)

Regarding Claim 46:

The references disclose A verification platform according to claim 32, characterized in that each transaction is constituted, at the level of each interface, by a request packet and one or more

associated response packets, wherein the values of the parameters and/or the transmission time constraints of the packets can be forced from the functional test program executed by the emulator of the environment, which appropriately translates all of said parameters during the transmission of the packets to the terminals of the software model of the design.

(Claim Interpretation. Process communications)

(Killian. Abstract. Figures 1, 6 , 8, and 10 and their corresponding descriptions. Column 2, Lines 12-23. Column 3, Lines 1-10.)

(Lin. Abstract. Figures 28-30 and their corresponding descriptions. Column 87, Line 50-64)

Regarding Claim 47:

The references disclose A verification platform according to claim 43 characterized in that each transaction is constituted, at the level of each interface, by a request packet and one or more associated response packets, wherein the values of the parameters and/or the transmission time constraints of the packets can be forced from the functional test program executed by the emulator of the environment, which appropriately translates all of said parameters during the transmission of the packets to the terminals of the software model of the design.

(Claim Interpretation. Process communications)

(Killian. Abstract. Figures 1, 6 , 8, and 10 and their corresponding descriptions. Column 2, Lines 12-23. Column 3, Lines 1-10.)

(Lin. Abstract. Figures 28-30 and their corresponding descriptions. Column 87, Line 50-64)

Conclusion

13. The prior art made of record is not relied upon because it is cumulative to the applied rejection. These references include:

i) **U.S. Patent No. 6,760,888.**

14. All Claims are rejected.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saif A. Alhija whose telephone number is (571) 272-8635. The examiner can normally be reached on M-F, 11:00-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571) 272-2279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAA

September 27, 2006

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